

REMARKS

Claim 9 has been amended to remove the antecedent basis problem.

Rejection of claims 1, 3-8, 11 and 13-16 under 35 U.S.C. 103(a) as unpatentable over Tayloe et al. in view of Widmer et al.:

Tayloe et al. discloses a packet switch, which receives LVDS inputs and produces LVDS outputs. Although Tayloe mentions SONET/SDH he does not describe how to process the SONET/SDH stream nor does he show "means for converting SONET/SDH signal streams to low voltage differential signal(s) and vice versa" contrary to what is stated in the Official Action. The data in Tayloe et al. is already encoded in LVDS on input lines 110 when presented to the device of Fig. 1 of Tayloe et al. (col. 2, lines 41-44). Similarly, after passing through switching network 105, the data is still encoded in LVDS on output lines 120 (col. 2, lines 43-44). The modems 130 in Tayloe et al. describe conversion from data format on LVDS to internal x1 format. There is no discussion on how SONET/SDH data is processed, how packets are extracted, or how packets are encoded onto the LVDS lines. It should be remembered that SONET/SDH is

an optical signal and is not inherently suitable for direct impression onto LVDS links. Some form of processing is required.

The Official Action also asserts that it was known at the date of the invention that 8B/10B transmission coding is desirable in a high speed transmission environment such as Tayloe et al. On page 443, Widmer describes the properties of the code itself, one of which is that some codes have even numbers of zeros and ones. There is no mention of how this property can be exploited in an application.

Applicant uses the positive and negative running disparity versions of the code having an even number of ones and zeros as two separate control characters (claim 4). These two disparity versions of the code carry two distinct elements of a time-division-multiplexing (TDM) stream. Page 446 of Widmer contains a description of digital sum variations over time. It does not deal with code interpretations.

Referring to claims 5 and 14, on page 4, paragraph 2, of the Official Action asserts that the combination of Tayloe and Widmer teaches the invention, including storing signals in a buffer and transferring the signals using a universal

frame pulse with a software programmable delay to allow transfer of one or more SONET/SDH signals over multiple links. Applicant is unable to locate any mention of frame pulses or programmable delays in col. 3 of Tayloe et al. Moreover, elements 140 and 180 of Tayloe et al. appear to be serial-to-parallel and parallel-to-serial conversion blocks. No mention is made of synchronization in Tayloe et al. as would be required if signals were transferred using a frame pulse. This may be because such conversion functions rarely require synchronization.

Referring to claim 6, the Official Action asserts that Widmer teaches error checking. Claim 6 refers to transparent in-band error reporting for errors detected at a SONET/SDH receiver. These are errors detected in the SONET/SDH stream, which are generated by the optical fiber and detected prior to encoding in 8b/10b characters. Claim 6 is concerned with reporting these errors from one end of the 8b/10b link to the other without disrupting traffic, not how to detect them. Widmer describes errors detected after encoding. Thus, the errors detected in Widmer are errors in the encoded stream; for example, a character chosen from the positive running disparity set instead of the negative set.

As per claims 7 and 15, the Official Action states that Widmer teaches a pseudo-random bit sequence pattern. A careful examination of Widmer discloses no mention of random patterns on pages 442-443.

Rejection of claims 1-8 and 11-16 under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. in view of Widmer et al.:

It is asserted that Johnson teaches a high density packet switch with high speed interfaces comprising transmitter and receiver including conversion means for converting SONET/SDH signal streams to low voltage differential signals and vice versa. Johnson's circuit receives optical SONET/SDH frames in each of four interface cards 31-34 which convert the optical signals to electrical ones. The electrical signals, still in SONET/SDH format are transmitted across the interfaces 46, etc. to the switching circuit 41. The switching circuit terminates the SONET frames by extracting the various data segments and organizing them according to whether they are formatted for ATM, IP or VT protocol. For example, data segments representing VT traffic are sent through interface 82 to

universal connector 72 to switching circuit card 102.

Switching circuit card 102 effects switching according to the VT protocol. (Switching circuit card 101 effects switching according to the ATM protocol with support from the APC circuit card 107).

Outgoing traffic from switching circuit card 102 is sent through connector 72 and interface 82 to switching circuit 41 where it is formatted into SONET frames. The resulting SONET frames are transmitted across the interface 51 to the line card 26. The multiplexer 31 converts the electrical signals corresponding to the SONET frames to optical format and transmits them across the communications path 16.

Essentially, Johnson receives SONET frames filled with data segments of various types, i.e., ATM, IP or VT, strips off the data segments, routes them to respective universal connectors having switching cards which utilize a particular protocol, i.e., ATM, IP or VT, and effects switching according to that protocol. The switched data segments are then sent back to the STS switch where they are formatted back into SONET frames and then converted back to optical signals before being transmitted over the communication paths 16-19.

Johnson does not disclose the use of 8B/10B coding, as recited in claim 1. In reference to claim 3, Johnson further does not map the 8B/10B control characters to ensure data transitions on serial links and to preserve DC balance. In fact, Johnson does not describe his data format or encoding methods of any of the communications paths in Fig. 1. As per claim 7, Johnson does not disclose the injection of pseudo-random sequences for system verification. As per claim 8, Johnson does not disclose using line code violations of 8B/10B characters to monitor error performance of serial links. As per claim 9, Johnson does not disclose overwriting unused SONET/SDH E1 and B1 bytes to form a pattern, which allows in-service monitoring of link functionality as well as monitoring of downstream cross-connect mis-configurations. As per claim 14, Johnson does not disclose use of a universal frame pulse with a software

programmable delay in order to allow transfer of one or more SONET/SDH signals over multiple links.

Respectfully submitted

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